IN THE CLAIMS

1-6. Canceled.

7. (New) A nonvolatile memory apparatus comprising:

a plurality of terminals including a clock terminal, a command terminal and a data terminal;

a central processing unit;

a first nonvolatile memory;

a second nonvolatile memory; and

a volatile memory,

wherein said clock terminal is capable of receiving a clock signal,

wherein said command terminal is capable of receiving commands for arbitrarily specifying any one of a plurality of operations and is capable of outputting a plurality of responses each of which corresponds to a received command,

wherein said data terminal is capable of receiving data and outputting data,

wherein said first nonvolatile memory stores a first program,

wherein said second nonvolatile memory stores data received from said data terminal and is further capable of storing a second program which is read out from said second nonvolatile memory to said volatile memory,

wherein said central processing unit reads out said first program from said first nonvolatile memory and executes said first program in response to receiving a first command received from said command terminal, and

wherein said central processing unit reads out said second program from said volatile memory and executes said second program, in response to receiving a second command received from said command terminal.

8. (New) A nonvolatile memory apparatus according to claim 7, wherein in response to receiving a data write command which is said first command, said central processing unit controls, by executing said first program, receiving of data from said data terminal to said volatile memory and storing data stored in said volatile memory to said second nonvolatile memory.

9. (New) A nonvolatile memory apparatus according to claim 8, wherein said volatile memory is assigned in a part of an address space which is accessible by said central processing unit.

10. (New) A nonvolatile memory apparatus according to claim 9, further comprising a second volatile memory, wherein said second volatile memory is assigned in another part of

said address space, and stores a vector table for storing branch addresses.

11. (New) A nonvolatile memory apparatus according to claim 8, wherein said second program is a compression program for compressing data stored in said second nonvolatile memory.

12. (New) A nonvolatile memory apparatus according to claim 11, further having a communication function, wherein said second program is used for said communication function.

13. (New) A nonvolatile memory apparatus comprising:

a program ROM;

a control circuit;

a volatile memory; and

a nonvolatile memory,

wherein said program ROM stores a first program which includes a data writing program,

wherein said nonvolatile memory is capable of storing file data executed said data writing program by said control circuit in response to a first command indicating a data writing function, and stores a second program therein, and

wherein said control circuit controls reading out of said second program to said volatile memory for operating a communication function in response to a second command.

14. (New) A nonvolatile memory apparatus according to claim 13, further comprising a data terminal, wherein said data terminal is capable of receiving data in parallel.

15. (New) A nonvolatile memory apparatus according to claim 14,

wherein said program ROM stores a vector table storing a plurality of program addresses each of which indicates said first program and said second program respectively,

wherein in response to receiving a command, said control circuit fetches a program address in said vector table corresponding to said received command.

16. (New) A nonvolatile memory apparatus according to claim 15, further comprising a second volatile memory, wherein said second volatile memory stores a management table for managing said nonvolatile memory.

17. (New) A nonvolatile memory apparatus according to claim 16, wherein said volatile memory and said second volatile memory are structured by SRAM.

18. (New) A nonvolatile memory apparatus according to claim 13, wherein said control circuit controls storing a program to said nonvolatile memory.

19. (New) A nonvolatile memory apparatus according to claim 13,

wherein said volatile memory is a part of a buffer memory,

wherein said buffer memory is capable of using temporarily stored data at data inputting and data outputting.